CAB-Q-S-P-xx M

40Gb/s QSFP+ Passive Breakout Copper Cable

Product Features

- ✓ Available in lengths of 1 to 5m
- ✓ Four-channel full-duplex active copper cable with breakout from QSFP+ to four SFP+
- ✓ Hot-pluggable QSFP +footprint
- ✓ RoHS compliant and Lead Free
- ✓ Power dissipation <0.1W (0~70℃)
- ✓ Commercial operating temperature optional
- ✓ Compliant with IEEE802.3ba, SFF-8436

Applications

- ✓ 40G Ethernet
- ✓ Infiniband 4X SDR DDR QDR
- ✓ 40G Telecom connections

Product Selection

Part Number	Lengths	Wire Size
CAB-Q-S-01M	1m	AWG28
CAB-Q-S-02M	2m	AWG28
CAB-Q-S-03M	3m	AWG28
CAB-Q-S-xxM	xxM	AWG28

*For availability of additional cable lengths, please contact LUXGLO.

Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883 Method 3015
- Immunity compatible with IEC 61000-4-3
- EMI compatible with FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B
- RoHS compliant with RoHS 2 (2011/65/EU)

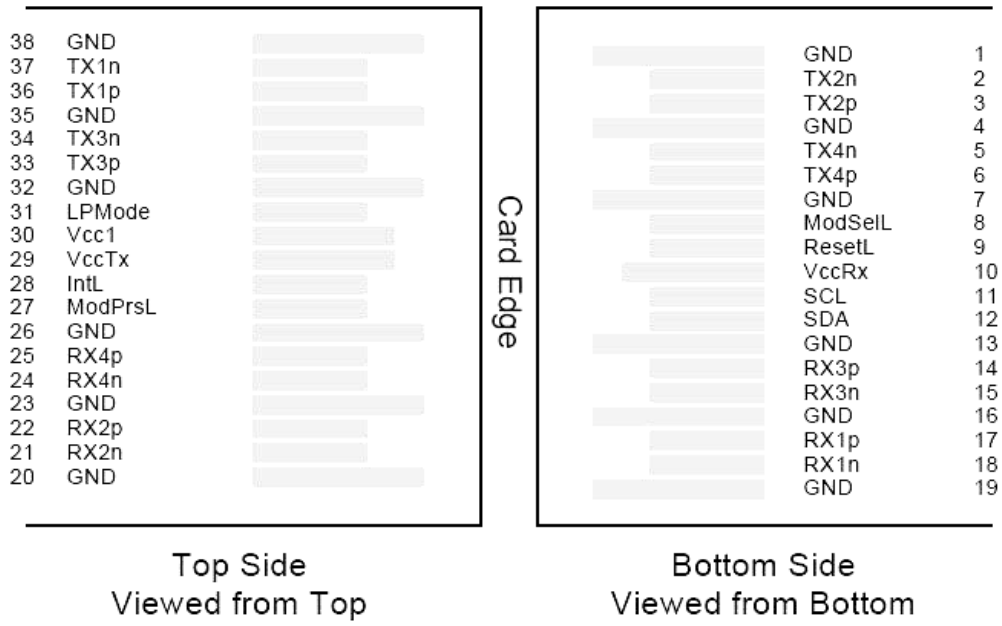
Pin Descriptions

QSFP+ End

Pin	Symbol	Name/Description	Ref.
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input, CML-I	
3	Tx2p	Transmitter Non-Inverted Data output, CML-I	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input, CML-I	
6	Tx4p	Transmitter Non-Inverted Data output, CML-I	
7	GND	GND	
8	ModSelL	The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the “High” state in the module	
9	ResetL	The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released.	
10	VccRx	+ 3.3V Power Supply Receiver	

11	SCL	2-Wire Serial Interface Clock	
12	SDA	2-Wire Serial Interface Data	
13	GND	GND	
14	Rx3p	Receiver Non-Inverted Data Output, CML-O	
15	Rx3n	Receiver Inverted Data Output, CML-O	
16	GND	GND	
17	Rx1p	Receiver Non-Inverted Data Output, CML-O	
18	Rx1n	Receiver Inverted Data Output, CML-O	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output, CML-O	
22	Rx2p	Receiver Non-Inverted Data Output, CML-O	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output, CML-O	
25	Rx4p	Receiver Non-Inverted Data Output, CML-O	
26	GND	Ground	
27	ModPrsL	Module Present, connect to GND	
28	IntL	The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The INTL pin is de-asserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of ‘0’ and the flag field is read.	
29	VccTx	+3.3 V Power Supply transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMode	The LPMode pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set software control bits (Address A0h, byte 93 bits 0,1).	
32	GND	Ground	

33	Tx3p	Transmitter Non-Inverted Data Input, CML-I	
34	Tx3n	Transmitter Inverted Data Output, CML-I	
35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input, CML-I	
37	Tx1n	Transmitter Inverted Data Output, CML-I	
38	GND	Ground	



Pin-out of Connector Block on Host Board

SFP+ End

Pin	Symbol	Name/Description	Note
1	VeeT	Transmitter Ground (Common with Receiver Ground)	1
2	TX Fault	Transmitter Fault. LVTTL-O	2
3	TX Disable	Transmitter Disable. Laser output disabled on high or open. LVTTL-I	3
4	SDA	2-Wire Serial Interface Data Line(Same as MOD-DEF2 in INF-8074i). LVTTL-I/O	2
5	SCL	2-Wire Serial Interface Data Line(Same as MOD-DEF2 in INF-	2

		8074i). LVTTL-I	
6	Mod_ABS	Module Absent, Connect to VeeT or VeeR in Module.	2
7	RS0	Rate Select 0, optionally controls SFP+ module receiver LVTTL-I	4
8	LOS	Loss of Signal indication. Logic 0 indicates normal operation. LVTTL-O	5
9	RS1	Rate Select 1, optionally controls SFP+ module transmitter. LVTTL-I	4
10	VeeR	Receiver Ground (Common with Transmitter Ground)	1
11	VeeR	Receiver Ground (Common with Transmitter Ground)	1
12	RD-	Receiver Inverted DATA out. AC Coupled. CML-O	
13	RD+	Receiver Non-inverted DATA out. AC Coupled. CML-O	
14	VeeR	Receiver Ground (Common with Transmitter Ground)	1
15	VccR	Receiver Power Supply	6
16	VccT	Transmitter Power Supply	6
17	VeeT	Transmitter Ground (Common with Receiver Ground)	1
18	TD+	Transmitter Non-Inverted DATA in. AC Coupled. CML- I	
19	TD-	Transmitter Inverted DATA in. AC Coupled. CML- I	
20	VeeT	Transmitter Ground (Common with Receiver Ground)	1

Notes:

1. Circuit ground is internally isolated from chassis ground.
2. T_fault is an open collector/drain output.which should be pulled up with a 4.7K – 10K Ohms resistor on the host board if intended for use.Pull up voltage should be between 2.0V to Vcc+0.3V.A high output indicates a transmitter fault caused by either the tx bias current or the tx output power exceeding the preset alarm thresholds.A low output indicates normal operation.In the low state,the output is pulled to <0.8V.
3. Laser output disabled on TX Disable >2.0V or open, enabled on TX Disable<0.8V.
4. Internally pulled down per SFF-8431 Rev4.1 .
5. LOS is open collector output. Should be pulled up with 4.7k – 10kohms on host board to a

voltage between 2.0V and 3.6V. Logic 0 indicates normal operation; logic 1 indicates loss of signal.

6. Internally connected

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		+4.0	V	
Storage Temperature	TS	-40		+85	°C	
Operating Humidity	RH	0		85	%	

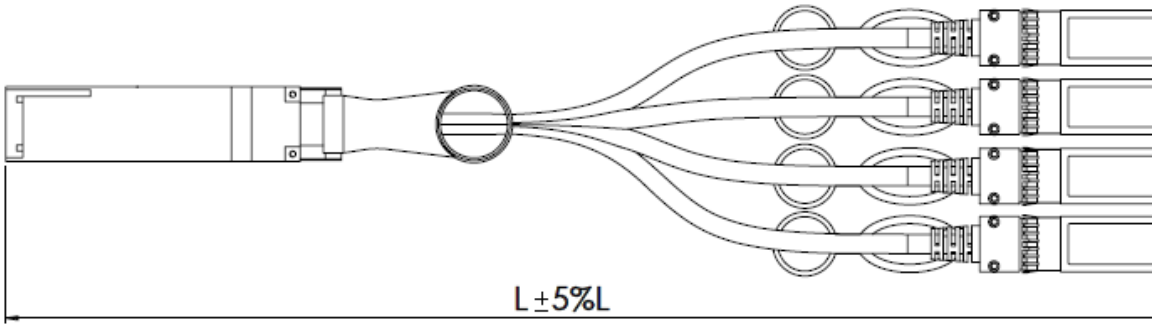
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Power Supply Voltage	Vcc	3.13	3.30	3.47	V	
Power Supply Current	Icc	-	-	1	A	QSFP+ End
				0.4	A	SFP+ End
Case Operating Temperature	Tc	0	-	+70	°C	
Bit Rate Each Lane	Br	1	-	11.3	Gbps	BER<1*10^{-12}

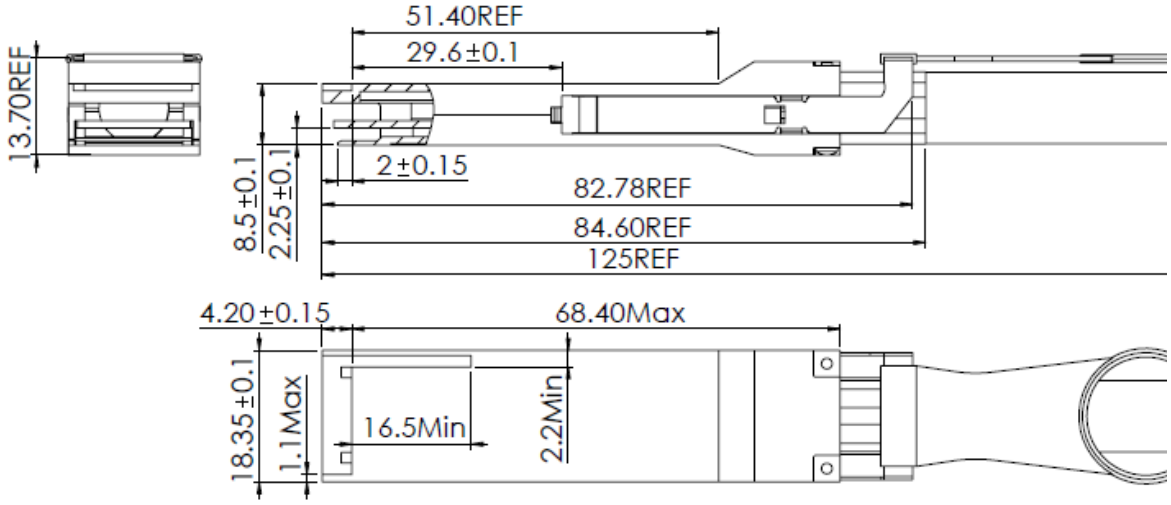
Electrical Characteristics (TOP=25°C, Vcc=3.3Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Input differential impedance	Rin	80	100	120	Ω	
Differential data input swing	Vin, pp	120	-	850	mV	
Receiver						
Output differential impedance	Rout	80	100	120	Ω	
Single ended data output swin	Vout'pp	300	-	850	mV	

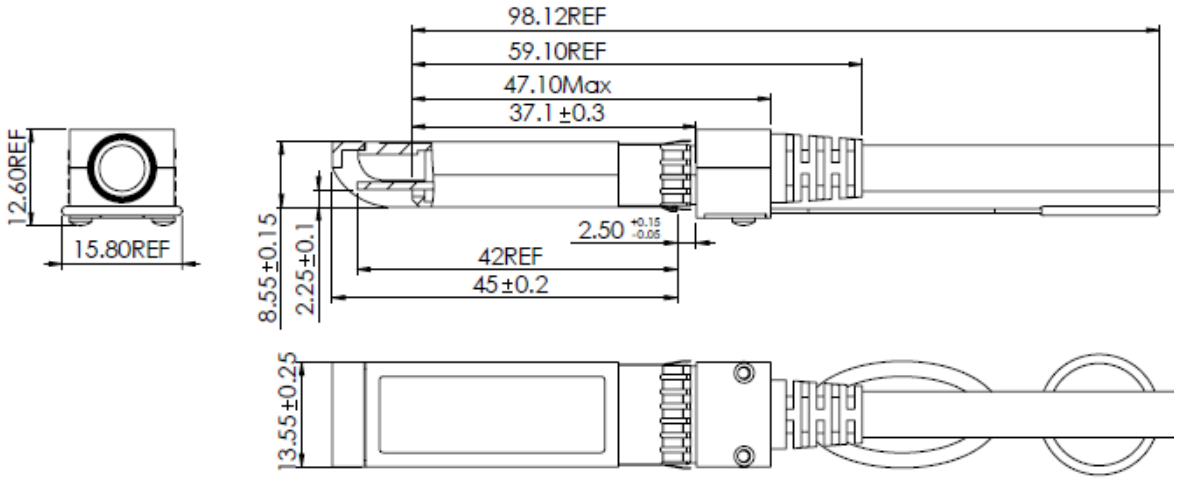
Mechanical Specifications



QSFP+ End



SFP+ End

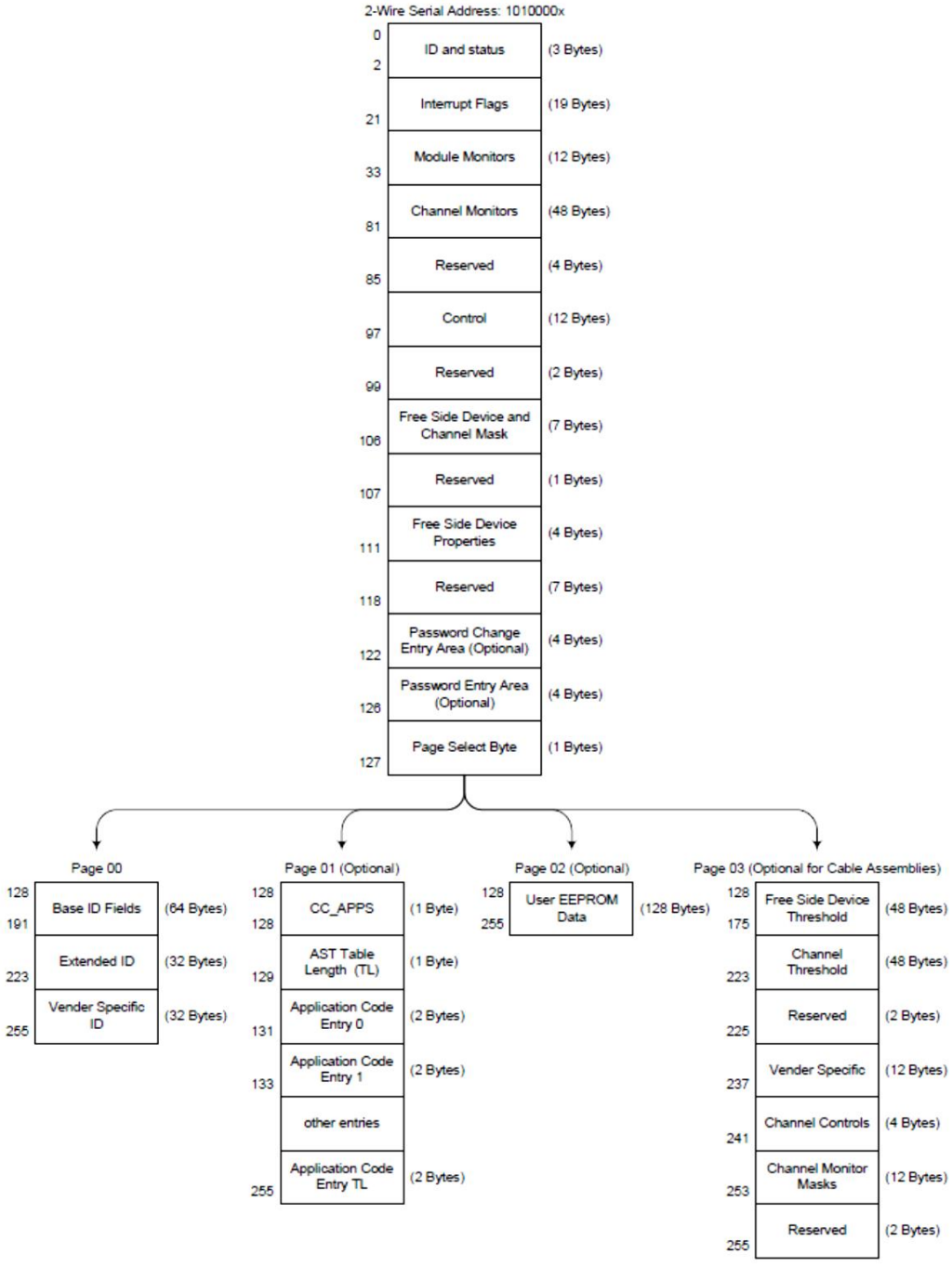


Length	Breakout point (measured from QSFP)	Breakout point (measured from SFP+)
1m	30cm	70cm
2m	60cm	1.4m
3m	1m	2m
4m	1m	3m
5m	2m	3m

Parameter	Symbol	Min	Typ	Max	Unit
Durability		100			cycle
Transceiver Insert Force		40			N
Transceiver Extraction Force		11.5			N
Transceiver Retention Force		90		170	N

EEPROM Information

EEPROM memory map specific data field description is as below:


2-Wire Serial Address: 1010000x
0
2
ID and status
(3 Bytes)
21
Interrupt Flags
(19 Bytes)
33
Module Monitors
(12 Bytes)
81
Channel Monitors
(48 Bytes)
85
Reserved
(4 Bytes)
97
Control
(12 Bytes)
99
Reserved
(2 Bytes)
106
Free Side Device and Channel Mask
(7 Bytes)
107
Reserved
(1 Bytes)
111
Free Side Device Properties
(4 Bytes)
118
Reserved
(7 Bytes)
122
Password Change Entry Area (Optional)
(4 Bytes)
126
Password Entry Area (Optional)
(4 Bytes)
127
Page Select Byte
(1 Bytes)
Page 00
128
191
Base ID Fields
(64 Bytes)
223
Extended ID
(32 Bytes)
255
Vender Specific ID
(32 Bytes)
Page 01 (Optional)
128
128
CC_APPS
(1 Byte)
129
AST Table Length (TL)
(1 Byte)
131
Application Code Entry 0
(2 Bytes)
133
Application Code Entry 1
(2 Bytes)
other entries
255
Application Code Entry TL
(2 Bytes)
Page 02 (Optional)
128
255
User EEPROM Data
(128 Bytes)
Page 03 (Optional for Cable Assemblies)
128
175
Free Side Device Threshold
(48 Bytes)
223
Channel Threshold
(48 Bytes)
225
Reserved
(2 Bytes)
237
Vender Specific
(12 Bytes)
241
Channel Controls
(4 Bytes)
253
Channel Monitor Masks
(12 Bytes)
255
Reserved
(2 Bytes)