CAB-Q-Q-P-xxM

40Gb/s QSFP+ Passive Copper Cable

■ Product Features

- ✓ Available in lengths of 1 to 5m
- ✓ 4 independent full-duplex channels up
  To 11.3Gbps data rate per wavelength
- ✓ Hot-pluggable QSFP +footprint
- ✓ RoHS compliant and Lead Free
- ✓ Power dissipation <0.1W (0~70℃)
- ✓ Commercial operating temperature optional
- ✓ Compliant with IEEE802.3ba, SFF-8436

■ Applications

- ✓ 40G Ethernet
- ✓ Infiniband 4X SDR DDR QDR
- ✓ 40G Telecom connections

■ Product Selection

Part Number	Lengths	Wire Size
CAB-Q-Q-P-1M	1m	AWG30
CAB-Q-Q-P-2M	2m	AWG30
CAB-Q-Q-P-3M	3m	AWG30
CAB-Q-Q-P-5M	Up To 5m	AWG26

*For availability of additional cable lengths, please contact LUXGLO.
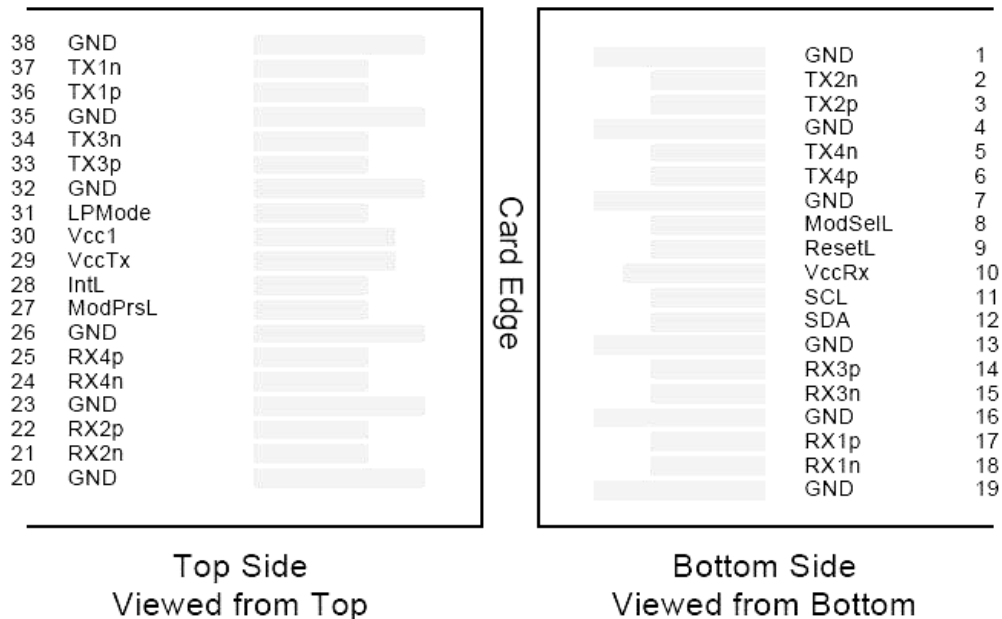
■ Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883 Method 3015
- Immunity compatible with IEC 61000-4-3
- EMI compatible with FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B
- RoHS compliant with RoHS 2 (2011/65/EU)

■ Pin Descriptions

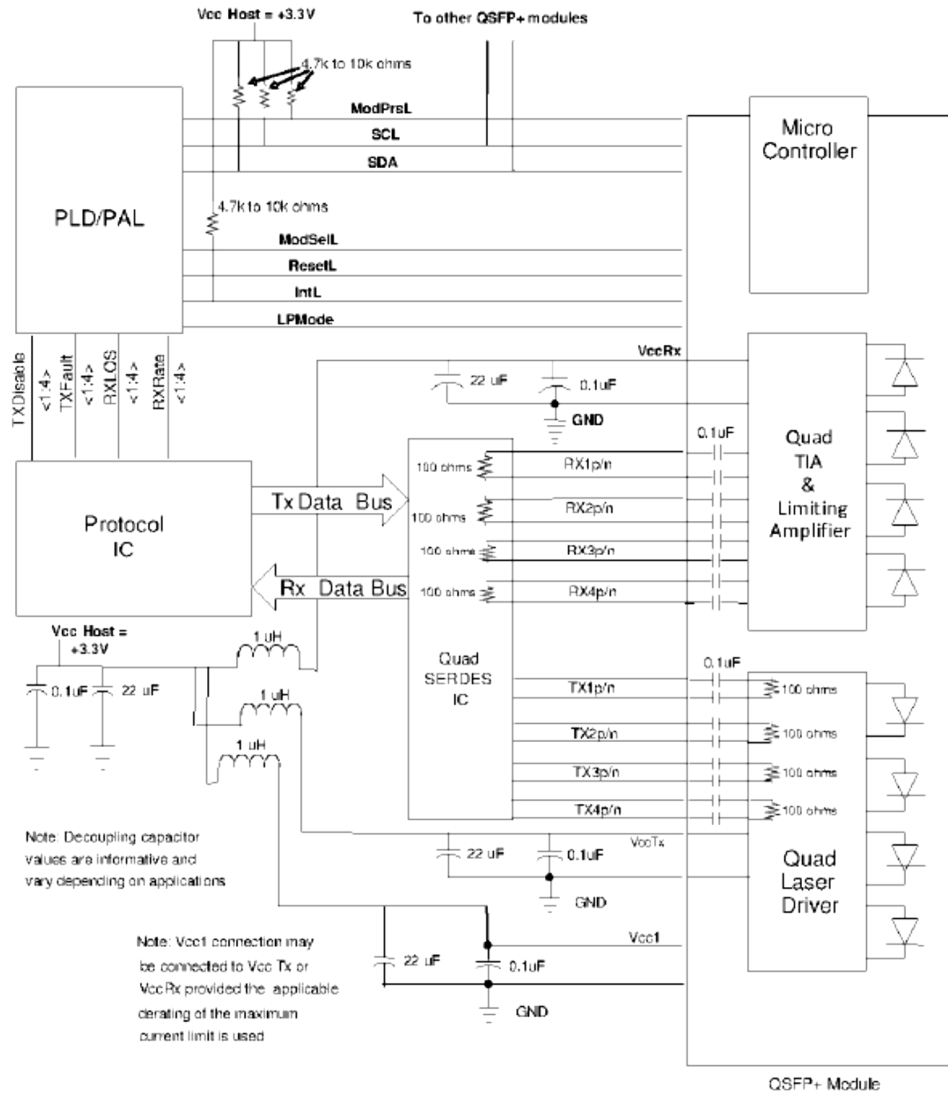| Pin	Symbol	Name/Description	Ref.
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input, CML-I	
3	Tx2p	Transmitter Non-Inverted Data output, CML-I	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input, CML-I	
6	Tx4p	Transmitter Non-Inverted Data output, CML-I	
7	GND	GND	
8	ModSelL	The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input	

		node must be biased to the "High" state in the module	
9	ResetL	The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released.	
10	VccRx	+ 3.3V Power Supply Receiver	
11	SCL	2-Wire Serial Interface Clock	
12	SDA	2-Wire Serial Interface Data	
13	GND	GND	
14	Rx3p	Receiver Non-Inverted Data Output, CML-O	
15	Rx3n	Receiver Inverted Data Output, CML-O	
16	GND	GND	
17	Rx1p	Receiver Non-Inverted Data Output, CML-O	
18	Rx1n	Receiver Inverted Data Output, CML-O	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output, CML-O	
22	Rx2p	Receiver Non-Inverted Data Output, CML-O	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output, CML-O	
25	Rx4p	Receiver Non-Inverted Data Output, CML-O	
26	GND	Ground	
27	ModPrsL	Module Present, connect to GND	
28	IntL	The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The INTL pin is de-asserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read.	
29	VccTx	+3.3 V Power Supply transmitter	

30	Vcc1	+3.3 V Power Supply	
31	LPMode	The LPMode pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set software control bits (Address A0h, byte 93 bits 0,1).	
32	GND	Ground	
33	Tx3p	Transmitter Non-Inverted Data Input, CML-I	
34	Tx3n	Transmitter Inverted Data Output, CML-I	
35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input, CML-I	
37	Tx1n	Transmitter Inverted Data Output, CML-I	
38	GND	Ground	

Top Side Viewed from Top		Bottom Side Viewed from Bottom	
38	GND	GND	1
37	TX1n	TX2n	2
36	TX1p	TX2p	3
35	GND	GND	4
34	TX3n	TX4n	5
33	TX3p	TX4p	6
32	GND	GND	7
31	LPMode	ModSelL	8
30	Vcc1	ResetL	9
29	VccTx	VccRx	10
28	IntL	SCL	11
27	ModPrsL	SDA	12
26	GND	GND	13
25	RX4p	RX3p	14
24	RX4n	RX3n	15
23	GND	GND	16
22	RX2p	RX1p	17
21	RX2n	RX1n	18
20	GND	GND	19

Card Edge

Pin-out of Connector Block on Host Board

■ Recommend Circuit Schematic

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Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		+4.0	V	
Storage Temperature	TS	-40		+85	°C	
Operating Humidity	RH	0		85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Power Supply Voltage	Vcc	3.13	3.30	3.47	V	
Power Supply Current	Icc	-	-	0.03	A	Commercial
Case Operating Temperature	Tc	0	-	+70	°C	Commercial
Bit Rate Each Lane	Br	1	-	11.3	Gbps	

Electrical Characteristics (TOP=25°C, Vcc=3.3Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Input differential impedance	Rin	80	100	120	Ω	
Receiver						
Output differential impedance	Rout	80	100	120	Ω	
S Parameters (10GSFP+Cu Cable Assembly Specifications at B' and C')						
Differential Output/Input Reflection Coefficient	SDDxx			$-12 + 2 \times SQRT(f)$	dB	1
				$-6.3 + 13 \times \log10(f/5.5)$	dB	2
Common Mode Output/Input Reflection Coefficient	SCCxx			$-7 + 1.6 \times f$	dB	3
				-3	dB	4

Note:

1: 0.01-4.1 GHz, reference differential impedance is 100 Ω. The dB value listed here are the same as dBe.

2: 4.1-11.1 GHz, reference differential impedance is 100 Ω. The dB value listed here are the same as dBe.

3: 0.01-2.5 GHz, reference differential impedance is 25 Ω. The dB value listed here are the same as dBe.

3: 2.5-11.1 GHz, reference differential impedance is 25 Ω. The dB value listed here are the same as dBe.

Mechanical Specifications
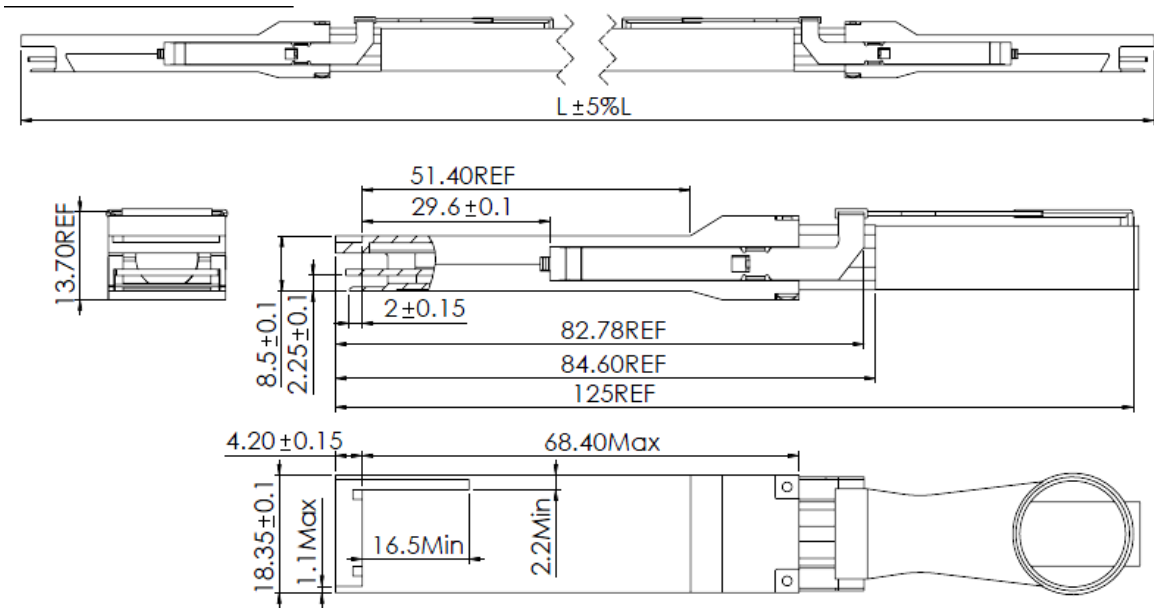
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Parameter	Symbol	Min	Typ	Max	Unit
Durability		100			cycle
Transceiver Insert Force		40			N
Transceiver Extraction Force		11.5			N
Transceiver Retention Force		90		170	N

◼ EEPROM Information

EEPROM memory map specific data field description is as below:

2-Wire Serial Address: 1010000x

Byte	Field	Size
0	ID and status	(3 Bytes)
2		
	Interrupt Flags	(19 Bytes)
21		
	Module Monitors	(12 Bytes)
33		
	Channel Monitors	(48 Bytes)
81		
	Reserved	(4 Bytes)
85		
	Control	(12 Bytes)
97		
	Reserved	(2 Bytes)
99		
	Free Side Device and Channel Mask	(7 Bytes)
106		
	Reserved	(1 Bytes)
107		
	Free Side Device Properties	(4 Bytes)
111		
	Reserved	(7 Bytes)
118		
	Password Change Entry Area (Optional)	(4 Bytes)
122		
	Password Entry Area (Optional)	(4 Bytes)
126		
	Page Select Byte	(1 Bytes)
127		

Page 00

Byte	Field	Size
128	Base ID Fields	(64 Bytes)
191		
	Extended ID	(32 Bytes)
223		
	Vender Specific ID	(32 Bytes)
255		

Page 01 (Optional)

Byte	Field	Size
128	CC_APPS	(1 Byte)
128	AST Table Length (TL)	(1 Byte)
129	Application Code Entry 0	(2 Bytes)
131	Application Code Entry 1	(2 Bytes)
133	other entries	
	Application Code Entry TL	(2 Bytes)
255		

Page 02 (Optional)

Byte	Field	Size
128	User EEPROM Data	(128 Bytes)
255		

Page 03 (Optional for Cable Assemblies)

Byte	Field	Size
128	Free Side Device Threshold	(48 Bytes)
175	Channel Threshold	(48 Bytes)
223	Reserved	(2 Bytes)
225	Vender Specific	(12 Bytes)
237	Channel Controls	(4 Bytes)
241	Channel Monitor Masks	(12 Bytes)
253	Reserved	(2 Bytes)
255		